A Battery-Balancing Nine-Level Inverter

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***Abstract*—In this paper, a nine-level inverter was designed and implemented to operate a battery balanced discharge system, which increases the ability of a stored energy utilization of a renewable energy sources. Also in this system a cascaded multilevel inverter with selective harmonic elimination and an algorithm to calculate the switching angles of a cascaded multilevel inverter minimizing the total harmonics distortion (THD) is proposed. The input of each level of cascaded multilevel inverter circuit is directly connected to a battery. Duty cycle of switch of each level is controlled to contain the ac output voltage with minimize total harmonic distortion. Additionally, the battery balanced discharged function is also achieved. Finally, an equivalent model block diagram of the proposed system to verify the feasibility and advantage by using Simulink software MATLAB. The stimulation results show that the proposed multilevel inverter with selective harmonic elimination and battery-balanced discharge function can eliminate harmonic and improve the cascaded battery-imbalanced problem effectively as we required.**

Index Terms—Cascaded Inverter, Minimum THD, Battery balanced discharge.

I.INTRODUCTION

In recent years, environmental concern and continuous depletion of fossil fuel reserves have spurred significant interest in renewable energy sources. The energy storage became a dominant factor in economic development with the widespread introduction of renewable sources. Unlike other common energy storage in prior use such as wood or coal, electricity must be used as it is being generated, or converted immediately into another form of energy such as potential, kinetic or chemical. Until recently electrical energy has not been converted and stored on a major scale, however new efforts to that effect began in the 21st century. An early solution to the problem of storing energy for electrical purposes was the development of the battery as an electrochemical storage device.

However, renewable energy sources such as wind turbine generators and photo- voltaic are intermittent in nature, and produce fluctuating active power. Interconnecting these intermittent sources to the utility grid at a large scale may affect the voltage/frequency control of the grid, and may lead to severe power quality issues. An energy storage system is indispensable for compensation which is a large capacity of the battery bank. In order to reduce energy loss in transmission lines and increase the overall battery capacity, the battery bank is usually connected in series for high voltage DC power supply. Batteries have previously been of limited use in electric power systems due to their relatively small capacity and high cost. However, since about the middle of the first decade of the 21st century, newer battery technologies have been developed that can now provide significant utility scale load-leveling capabilities some of which, as of 2013, showed promise of being competitive with alternative methods.

A similar possible solution to deal with the intermittency issue of solar and wind energy is found in the capacity. This result is smaller storage capacity and shorter cycle life. Therefore, the power conversion system requires a battery balancing circuit as shown in fig.1, to adjust each battery voltage to be equal.

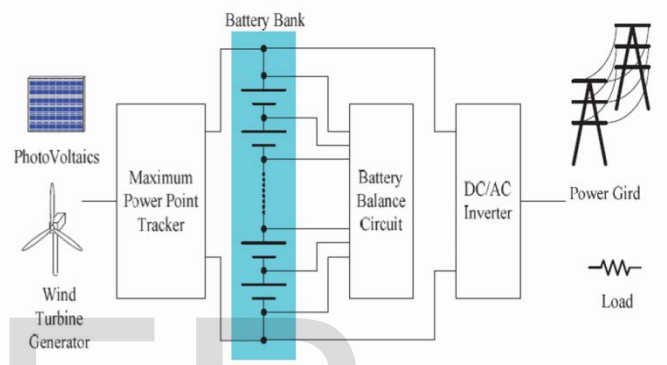

Fig. 1 Renewable energy systems

The battery balancing strategies can be categorized into three approaches:

1. Balancing by providing additional charging current for each battery until the voltage of each unit reaches a set threshold. But this process is either the battery subjected to over charged condition or the switching device is subjected to high voltage stress.
2. 0Balancing by individually draining excessive current from battery which voltage is above a set threshold back to the main charging bus. This process needs the high voltage conversion ratio of converter, which will cause

   the system efficiency decrease and the high voltage stress on the switching devices.
3. Balancing by allowing the current to flow both in and out off the batteries until the voltage of each reaches a set threshold. This process is uses the switching circuit of control the battery energy, which transfers the high capacity battery energy into the low capacity battery by a capacitor or a inductor storage of energy temporarily. It will increase the energy loss in transmission lines and switch components.

However, an additional battery balancing circuit not only increase circuit complex and cost .but also reducing efficiency. To solve this problem, a cascaded multilevel inverter with selective harmonic elimination and batterybalancing discharge function is proposed. Multilevel cascade converters are an attractive topology for medium-voltage high power applications. Since it is simple and modular in structure, and can reach medium/high voltages with low voltage/current harmonics without using step-up

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transformers or switching devices connected in series. In this paper, the input of each level of cascaded multilevel inverter circuit is directly connected to a battery. The duty cycle of each level is controlled to contain the ac output voltage with minimize total harmonic distortion. Additionally, the batterybalancing discharge function is also achieved. Finally, a prototype is realized to verify the feasibility and excellent performance.

II.MULTI-LEVEL INVERTER

A multilevel inverter is more recent and popular type of power electronic converter that synthesizes a desired output voltage from nine levels of dc voltages as inputs. If sufficient number of dc sources is used, a nearly sinusoidal voltage waveform can be synthesized. In comparison with the hard-switched two-level pulse width modulation inverter, multilevel inverter offers several advantages such as, its capabilities to operate at high voltage with lower dv/dt per switching, high efficiency and low electromagnetic interference [1]-[4].

To synthesize multilevel output ac voltage using different levels of dc inputs, semiconductor devices must be switched on and off in such a way that desired fundamental is obtained with minimum harmonic distortion. The commonly available switching technique is selective harmonic elimination (SHE) method at fundamental frequency, for which transcendental equations characterizing harmonics are solved to compute switching angles [2], [3]. It is difficult to solve the SHE equations as these are highly nonlinear in nature and may produce simple, multiple, or even no solutions for a particular value of modulation index.

A big task is how to get all possible solution sets where they, exist using simple and less computationally complex method. Once these solution sets are obtained, the solutions having least THD are chosen. In [4]-[6], iterative numerical techniques have been implemented to solve the SHE equations producing only one solution set, and even for this a proper initial guess and starting value of modulation index for which solutions exist are required. In [7], [8], theory of resultants of polynomials and the theory of symmetric polynomials has been suggested to solve the polynomial equations obtained from the transcendental equations.

A difficulty with these approaches is that for several Hbridges connected in series, the order of the polynomials become very high thereby making the computations of the solutions of these polynomials very complex. Optimization technique based on Genetic Algorithm (GA) was proposed for computing switching angles for 9-level inverter in [9].

The implementation of this approach requires proper selection of certain parameters such as population size, mutation rate etc, thereby its implementation becomes also difficult for higher level inverters. To circumvent above problems, in this paper the application of the NewtonRaphson method for solving these equations is proposed. The proposed technique is implemented in such a way that all possible solutions for any number of H-bridges connected in series are computed for any arbitrary initial guess with negligible computational effort. A complete analysis for an 9-level inverter using four H-bridges per phase in series is presented, and it is shown that for a range of modulation index, switching angles can be computed to produce the desired fundamental voltage V1 = (s 4Vdc/) while eliminating 5^{th},7^{th} ,11^{th} and 13^{th} harmonic components.

Cascade Multilevel Inverter

Cascade Multilevel Inverter (CMLI) is one of the most important topology in the family of multilevel and multipulse inverters. It requires least number of components with compare to diode-clamped and flying capacitors type multilevel inverters and no specially designed transformer is needed as compared to multi-pulse inverter. It has modular structure with simple switching strategy and occupies less space [1], [3]. The CMLI consists of a number of H-bridge inverter units with separate dc source for each unit and is connected in cascade or series as shown in Fig. 2. Each Hbridge can produce three different voltage levels: +Vdc, 0, and –Vdc by connecting the dc source to ac output side by different combinations of the four switches S1, S2, S3, and S4.

The ac output of each H-bridge is connected in series such that the synthesized output voltage waveform is the sum of all of the individual H-bridge outputs. By connecting the sufficient number of H-bridges in cascade and using proper modulation scheme, a nearly sinusoidal output voltage waveform can be synthesized. The number of levels in the output phase voltage is 2s+1, where s is the number of H-bridges used per phase. Fig. 3 shows a 9-level output phase voltage waveform using four H-bridges. The magnitude of the ac output phase voltage is given by *van=va1+va2+va3+va4*[2].

III. PWM

Multicarrier phase disposition PWM scheme is employed in the generation of the gating signals. Basic principle of the proposed switching strategy is to generate gate signals by comparing the rectified sinusoidal modulating/reference signal, at the fundamental frequency, with four triangular carrier waves having higher switching frequency and inphase, but different offset voltages. In practice, carrier to

Table 1 Output voltage according to the switches on-off conditions

v_o	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_A	S_B
V_S	off	on	off	off	off	on	off	off	on	Off
$2V_S$	on	on	off	off	off	on	off	off	off	Off
$3V_S$	on	on	off	off	off	on	off	off	off	On
$4V_S$	on	on	off	off	on	on	off	off	off	Off
0	off	on	off	off	off	on	off	off	off	off
0	off	off	off	on	off	off	off	on	off	off
$-V_S$	off	off	on	off	off	off	on	off	on	off
$-2V_S$	off	off	on	on	off	off	on	off	off	off
$-3V_S$	off	off	on	on	off	off	on	off	off	on
$-4V_S$	off	off	on	on	off	off	on	on	off	off

Range of M_a	θ_1	θ_2	θ_3	θ_4	θ_5	θ_6	θ_7	θ_8	θ_9	θ_{10}	θ_{11}	θ_{12}
$M_a<0.25$	$(\pi/2)$	$(\pi/2)$	$(\pi/2)$	$(\pi/2)$	$(\pi/2)$	$(\pi/2)$	$(5\pi/2)$	$(5\pi/2)$	$(5\pi/2)$	$(5\pi/2)$	$(5\pi/2)$	$(5\pi/2)$
$0.25< M_a \leq 0.5$	$\sin^{-1}(A_1/A_m)$	$(\pi/2)$	$(\pi/2)$	$(\pi/2)$	$(\pi/2)$	$\pi-\theta_1$	$\Pi+\theta_1$	$(5\pi/2)$	$(5\pi/2)$	$(5\pi/2)$	$(5\pi/2)$	$2\pi-\theta_1$
$0.5< M_a \leq 0.75$	$\sin^{-1}(A_1/A_m)$	$\sin^{-1}(A_2/A_m)$	$(\pi/2)$	$(\pi/2)$	$\pi-\theta_2$	$\pi-\theta_1$	$\pi+\theta_1$	$\pi+\theta_2$	$(5\pi/2)$	$(5\pi/2)$	$2\pi-\theta_2$	$2\pi-\theta_1$
$M_a>0.75$	$\sin^{-1}(A_1/A_m)$	$\sin^{-1}(2A_2/A_m)$	$\sin^{-1}(3A_3/A_m)$	$\pi-\theta_3$	$\pi-\theta_2$	$\pi-\theta_1$	$\pi+\theta_1$	$\pi+\theta_2$	$\pi+\theta_3$	$2\pi-\theta_3$	$2\pi-\theta_2$	$2\pi-\theta_1$

Table 2 Range of modulation index and the corresponding values of the phase angle displacement

fundamental frequency ratio of 40 is adopted for better performance of this multilevel PWM scheme [10]. For one cycle of the fundamental frequency, the proposed multilevel inverter operates through eight modes. Fig. 3 illustrates the per unit output voltage waveform for one cycle. The eight modes are described as follows

Mode 1 := 0 , vt ≤ u1 and u6 ≤ vt ≤ p;
Mode 2 := u1 ≤ vt ≤ u2 and u5 ≤ vt ≤ u6
Mode 3 := u2 , vt ≤ u3 and u4 ≤ vt ≤ u5;
Mode 4 := u3 ≤ vt ≤ u4
Mode 5 := p , vt ≤ u7 and u12 ≤ vt ≤ 2p;
Mode 6 := u7 ≤ vt ≤ u8 and u11 ≤ vt ≤ u12
Mode 7 := u8 , vt ≤ u9 and u10 ≤ vt ≤ u11;
Mode 8 := u9 ≤ vt ≤ u10

The phase angle θ, depends on the modulation index, Ma[11]

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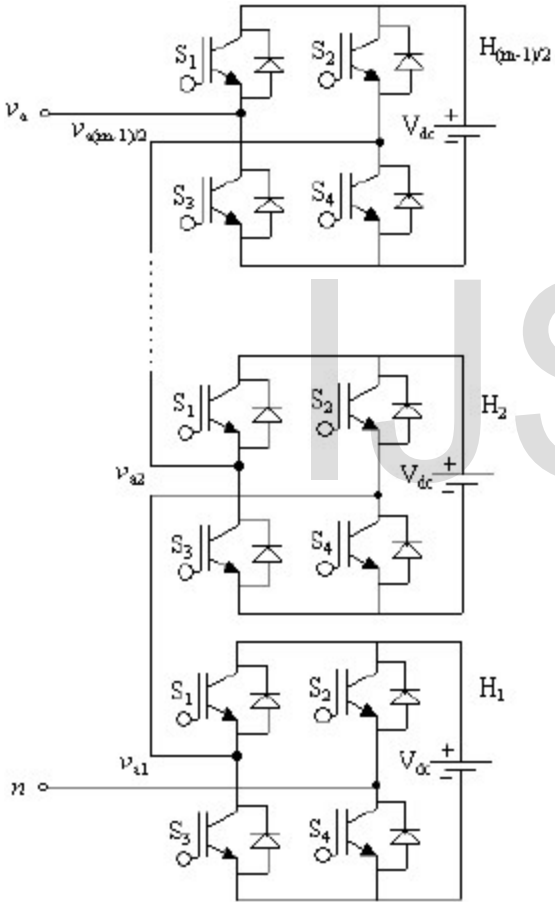

Fig. 2 H-Bridge Cascade Multilevel Inverter

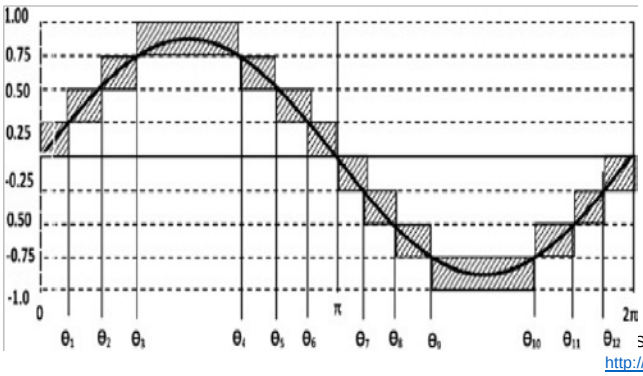

Fig. 3 9-level output voltage and switching angles

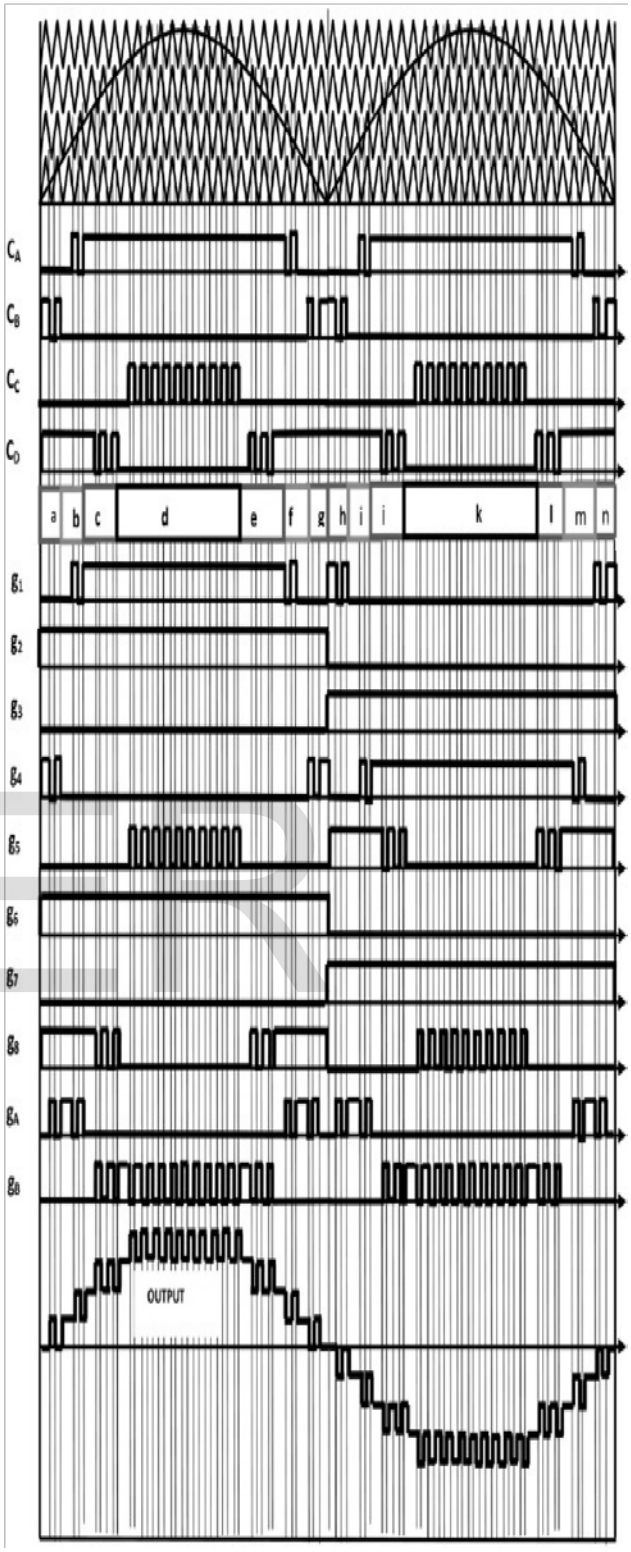

Fig. Output voltage waveform and

IV.SELECTIVE HARMONIC ELIMINATION

There are many popular methods are used to reduce the harmonics in order to get an effective results. The popular methods for high switching frequency are Sinusoidal PWM and Space Vector PWM. For low switching frequency methods are space vector modulation and selective harmonic elimination. The SPWM technique has disadvantage that it cannot completely eliminate the low order harmonics. Due to this it cause loss and high filter requirement is needed. In Space Vector Modulation technique cannot be applied for unbalanced DC voltages.

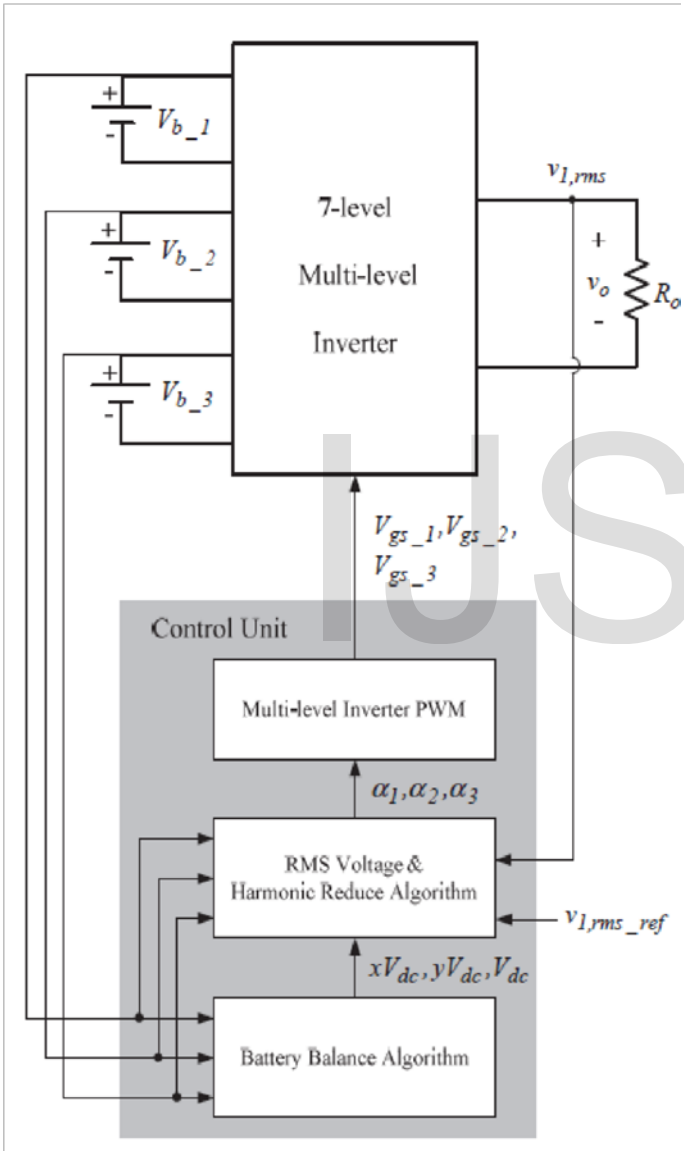

Fig. 5 System block diagram

SHE PWM technique uses many mathematical methods to eliminate specific harmonics such as 5^{th}, 7^{th}, 11^{th}, and 13^{th} harmonics. The popular Selective Harmonic Elimination method is also called fundamental switching frequency based on harmonic elimination Theory. As shown in Fig.3, a multilevel converter can produce a quarter-wave symmetric stepped voltage waveform synthesized by several DC voltages. Multilevel inverters provide a less THD than other inverters and it can improve with more levels added. One of the drawbacks is the calculation of the switching angles since the more levels are needed, more angles must be calculated and more time is spent in calculation. Fig. 3 shows a multilevel inverter output for nine steps. Multilevel inverters provide a less THD than other inverters and it can improve with more levels added. One of the drawbacks is the calculation of the switching angles since the more levels are needed, more angles must be calculated and more time is spent in calculation. Fig. 3 shows a multilevel inverter output for nine steps. One of the most used techniques for finding the switching angles is to use the rms of harmonic each battery output voltage components and the switching voltage components coefficients to eliminate some harmonics. The number of harmonics to be eliminated is equal to the number of switching angles to be calculated minus one, with this technique A computer program can be used to find the switching angles for the minimum THD using the same equation, nevertheless the amount of time of calculation increases with the number of angles. Calculation of THD requires computing of *p* cosines, two square roots, 2*p* summations, *p*+2 multiplications, and one division, where p is the number of angles to be calculated. Calculation of the minimum THD depends on angle resolution. For one degree resolution the first angle goes from 1° to 89° in steps of 1°, the second angle goes from 2° to 89° and so on, so that for *p* angles it is needed (90-n)/*p1* where *p1* in the range of 1 to *p* THD calculations. checks for the minimum THD in all possible values o∏ f each

For example, for two angles with one degree resolution it is needed 3,916 THD calculations, assuming the program angle. For three angles with the same resolution it is needed 113,564 THD calculations. The flowchart of the program is shown in Fig. 6. The more switching angles are needed, the more for loops must be nested and the program can spent a lot of time running. That is why the increment (Inc) is a key to find first a close value for switching angles and then modify the limit values of each loop, that is, angle i that goes from aiL to aiH, its limit values. The increment (Inc) starts with a large value, say 6 in the all range of the angles, from 0 to 90 degrees.

The first run of the program gives the seeds or close angle values for the minimum THD. For example, for p= 5 and Inc= 6 the first run of the program gives 7°, 14°, 27°, 40° and 59°. This first run needs 2002 THD calculations, less than is needed for two angles calculation. The new limit values can be calculated from the Inc value as aiL= aix-Inc/2 and aiH= aix+Inc/2, where aix is the new value of the angle i. For this example the limit values are (4, 10), (11, 17), (24, 30), (37, 43) and (56, 62). Closer angles for the real minimum THD can be found with Inc equal to 1. In this case the second run of the program gives 6°, 17°, 29°, 42° and 60°, and the new limit values for Inc equal to 0.1 are (5.5, 6.5), (16.5, 17.5), (28.5, 29.5), (41.5, 42.5) and (59.5, 60.5).

The second run of the program needs 7,776 THD calculations. The third run of the program with these values gives the angles in table 3 for three to fifteen levels.

SWITCHING ANGLES FOR MINIMUM THD IN MULTILEVEL INVERTERS

Levels	THD (%)	α_1	α_2	α_3	α_4	α_5	α_6	α_7
3	28.96	23.2°						
5	16							
7	11							
9	8							
11	7							
13	6							
15	5							

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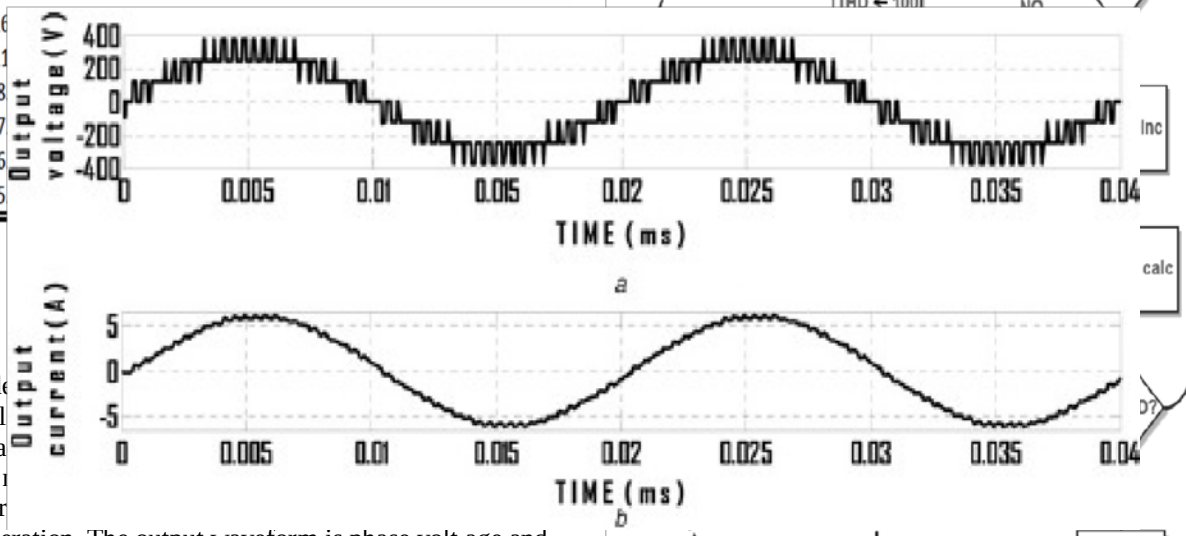

Fig. 7 Simulation results of output voltage & current

In orde
multilevel
out in a
proposed
scheme pr
pulse generation. The output waveform is phase volt age and it comprises nine levels. The SHE-PWM technique is used to reduce the odd harmonics. The nine level inverter o utput is shown below in the Fig. 7

Fig.6 Flow chart for switching angle calculation

VI.CONCLUSION

Presented in this paper is a new configuration for cascaded multilevel inverter. The operational principles, modulation scheme and switching functions have been analyzed in detail. The proposed multilevel inverter exhibited the behaviors of 3-, 5- and 7-level inverters earlier reported, in addition to the characteristics herein. By controlling the modulation index, the desired number of levels of the inverter's output voltage has been achieved.

In this project, a cascaded multilevel inverter with selective harmonic elimination and battery-balanced discharge function is succeeding proposed. The input of each level of cascaded multilevel inverter circuit is directly connected to a battery. Duty cycle of switch of each level is controlled to contain the ac output voltage with minimize total harmonic distortion. The simulation system results show that the proposed multilevel inverter with selective harmonic elimination and battery-balanced discharge function can eliminate harmonic and improve the cascaded batteryimbalanced problem effectively as we wanted.

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